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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LE, JOHN H	

ART UNIT	PAPER NUMBER
2863	

DATE MAILED: 12/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/672,246	KIM, JUNG PILL	
	Examiner	Art Unit	
	John H Le	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,3-5 and 15-17* is/are allowed.

6)☒ Claim(s) *6-9,11-14,18 and 19* is/are rejected.

7)☒ Claim(s) *2,10 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/25/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 2, 7, 8, and 18 are objected to because of the following informalities:

Claim 2, lines 3-4, "first comparator" should change to –second comparator--.

Claim 7, lines 3-4, "first comparator" should change to –second comparator--.

Claim 8, line 4, "first comparator" should change to –second comparator--.

Claim 18, line 7, "first reference" should change to –second reference--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 6-9, 11, 13, 18, and 19 are rejected under 35 U.S.C. 103(a) as obvious over Chesnut et al. (USP 4,302,663).

Regarding claims 6 and 18, Chesnut et al. disclose temperature sensing circuit (80) comprising: a first and a second comparator (84, 94) each configured to receive a sense voltage (the voltage input at terminals 86, 96) that is indicative of a sensed temperature (e.g. Col.6, lines 10-21); a first temperature reference

circuit (82) having a plurality of first reference voltages coupled to the first comparator (84) such that the plurality of first reference voltages are alternately compared with the sense voltage (e.g. Col.6, lines 10-30); a first trimmer (potentiometer 126) coupled to the first temperature reference circuit (82), the first trimmer being independently adjustable to adjust the plurality of first reference voltages (e.g. Col.5, lines 24-37, 59-64).

Regarding claims 7 and 19, Chesnut et al. disclose the trimmer (potentiometer 126) is adjustable to correct for input offset voltage in the comparator (e.g. Col.5, lines 24-37, 59-64).

Regarding claim 8, Chesnut et al. disclose the first trimmer is resistor that is adjustable to correct for input offset voltage in the first comparator (e.g. Col.5, lines 24-37, 59-64).

Regarding claim 9, Chesnut et al. disclose the first trimmer is potentiometer that has adjustable resistance (e.g. Col.5, lines 24-37, 59-64).

Regarding claim 11, Chesnut et al. disclose a sensing device configured to sense the sensed voltage that varies with changes in temperature at the sensing device (e.g. Col.6, lines 10-30).

Chesnut et al. discloses the claimed invention except for a second temperature reference circuit coupled to the second comparator for alternately comparing a plurality of first reference voltages with the sense voltage; and a second trimmer coupled to the second temperature reference circuit for independently adjusting the plurality of second reference voltages.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to include a second temperature reference circuit coupled to the second comparator for alternately comparing a plurality of first reference voltages with the sense voltage; and a second trimmer coupled to the second temperature reference circuit for independently adjusting the plurality of second reference voltages since Chesnut et al. teach a first temperature reference circuit (82) having a plurality of first reference voltages coupled to the first comparator (84) such that the plurality of first reference voltages are alternately compared with the sense voltage (e.g. Col.6, lines 10-30); a first trimmer (potentiometer 126) coupled to the first temperature reference circuit (82), the first trimmer being independently adjustable to adjust the plurality of first reference voltages (e.g. Col.5, lines 24-37, 59-64). It has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.

4. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chesnut et al. (USP 4,302,663) in view of Bradenbaugh (USP 6,455,820).

Regarding claim 12, Chesnut et al. fail to disclose a logic circuit configured to receive an output signal from the comparator.

Bradenbaugh discloses a logic circuit 121 configured to receive an output signal from the comparator 113 (Fig.2, Col.6, lines 54-59).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a logic circuit 121 as taught by Bradenbaugh in a control system for heater of Chesnut et al. for the purpose of providing controlling

the thyristor in response to signals from the temperature sensing device and the temperature set point device (Bradenbaugh, Col.3, lines 30-33).

5. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chesnut et al. (USP 4,302,663) in view of Simcoe et al. (USP 4,228,511).

Regarding claim 14, Chesnut et al. fail to disclose the temperature sensing circuit configured to be integrated into a random access memory device.

Simcoe et al. disclose the temperature sensing circuit configured to be integrated into a random access memory device (Col.11, lines 20-24).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the temperature sensing circuit configured to be integrated into a random access memory device as taught by Simcoe et al. in a control system for heater of Chesnut et al. for the purpose of providing an integral power deferral and thermostatic control system for the ambient temperature conditioning means (Simcoe et al., Col.2, lines 54-56).

Allowable Subject Matter

6. Claims 1, 3-5, and 15-17 are allowed.

Claims 10 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 1, none of the prior art of record teaches or suggests the combination of a random access memory device including a temperature sensing

circuit, the temperature sensing circuit comprising: a sensing device configured to hold a sensed voltage that varies with changes in temperature at the sensing device; a first comparator configured to receive the sensed voltage from the sensing device, the first comparator generating a first output signal; a second comparator configured to receive the sensed voltage from the sensing device, the second comparator generating a second output signal; a logic circuit configured to receive the first and second output signals; a first temperature reference circuit having a plurality of first reference voltages; a second temperature reference circuit having a plurality of second reference voltages; a first switch circuit coupled between the first temperature reference circuit and the first comparator, the first switch circuit controlled by the logic circuit such that a first reference voltage is applied to the first comparator; a second switch circuit coupled between the second temperature reference circuit and the second comparator, the second switch circuit controlled by the logic circuit such that a second reference voltage is applied to the second comparator; a first trimmer coupled to the first temperature reference circuit, the first trimmer being adjustable to adjust the first reference voltage; and a second trimmer coupled to the second temperature reference circuit, the second trimmer being adjustable to adjust the second reference voltage. It is these limitations as they are claimed in the combination with other limitations of claim, which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Regarding claim 10, none of the prior art of record teaches or suggests the combination of a temperature sensing circuit comprising: a first and a second comparator each configured to receive a sense voltage that is indicative of a sensed temperature; a first temperature reference circuit having a plurality of first reference voltages coupled to the first comparator such that the plurality of first reference voltages are alternately compared with the sense voltage; a second temperature reference circuit having a plurality of second reference voltages coupled to the second comparator such that the plurality of second reference voltages are alternately compared with the sense voltage; a first trimmer coupled to the first temperature reference circuit and a second trimmer coupled to the second temperature reference circuit, the first and second trimmers being independently adjustable to adjust the plurality of first and second reference voltages, wherein the first and second trimmers are multiple resistors that may be removed and added to the trimmers in order to provide adjustable resistance. It is these limitations as they are claimed in the combination with other limitations of claim, which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Regarding claim 13, none of the prior art of record teaches or suggests the combination of a temperature sensing circuit comprising: a first and a second comparator each configured to receive a sense voltage that is indicative of a sensed temperature; a first temperature reference circuit having a plurality of first reference voltages coupled to the first comparator such that the plurality of first reference voltages are alternately compared with the sense voltage; a second

temperature reference circuit having a plurality of second reference voltages coupled to the second comparator such that the plurality of second reference voltages are alternately compared with the sense voltage; a first trimmer coupled to the first temperature reference circuit and a second trimmer coupled to the second temperature reference circuit, the first and second trimmers being independently adjustable to adjust the plurality of first and second reference voltages; and a first switch circuit coupled between the first temperature reference circuit and the first comparator and a second switch circuit coupled between the second temperature reference circuit and the second comparator, the first and second switch circuits controlled by the logic circuit such that the plurality of first and second reference voltages are alternately compared with the sense voltage. It is these limitations as they are claimed in the combination with other limitations of claim, which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Regarding claim 15, none of the prior art of record teaches or suggests the combination of a method of decreasing current consumption in a dynamic memory device, wherein the method including the steps of: providing a semiconductor memory device with a temperature sensing circuit; periodically refreshing the memory device at a refresh rate; sensing the temperature of the dynamic memory device with the temperature sensing circuit and producing a corresponding sensed temperature voltage; providing a first reference voltage; comparing the sensed temperature voltage with the first reference voltage using a first comparator with a first offset voltage; providing a second reference

voltage; comparing the sensed temperature voltage with the second reference voltage using a second comparator with a second offset voltage; determining whether the sensed temperature voltage is within the first and second reference voltages; adjusting the first reference voltage to balance the first input offset voltage of the first comparator; and adjusting the second reference voltage to balance the second input offset voltage of the second comparator. It is these limitations as they are claimed in the combination with other limitations of claim, which have not been found, taught or suggested in the prior art of record, that make these claims allowable over the prior art.

Other Prior Art

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Beer et al. (USP 6,612,738) disclose a method for determining the temperature of a semiconductor chip and semiconductor chip with temperature measuring configuration.

Aslan et al. (USP 6,149,299) disclose an apparatus and method for directly measuring the operating temperature of a semiconductor device.

Contact Information

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John H Le whose telephone number is 571-272-2275. The examiner can normally be reached on 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E Barlow can be reached on 571-272-2269. The fax

phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John H. Le

Patent Examiner-Group 2863

December 10, 2004

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